Jointwave H.264 Encoder Live Demo User Guide

Xilinx CVK by TED Edition

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1. INTRODUCTION

This Jointwave H.264 Encoder Live Demo provides an evaluation version of E240, E340, E440, E540, and E640 demo on Xilinx's standard FPGA development board (Spartan-6 FPGA Consumer Video Kit by TED, where the main board is TS-6S-LX150T).

Demos on TED inrevium TS-6S-LX150T board:

Encoder Model	Profile	GOP	1920x1080p FPS	1280x720p FPS
E640	Main	I+P	0 to 30	0 to 72
E540	Baseline	I+P	0 to 30	0 to 72
E440	Main	I+P	0 to 30	0 to 72
E340	Main	I only	0 to 30	0 to 72
E240	Baseline	I only	0 to 30	0 to 72

There are several limitations of evaluation version comparing with formal version:

- Logo : The evaluation encoder added a "*Jointwave*" logo on right-bottom position of the encoded video
- Time Limitation: The evaluation encoder can work continuously for *three to five hours* after power up or reset, then the encoder might stop working or the output data might be corrupted, Pressing an user button on the FPGA board to reset would resume the encoding to work continuously for another four hours.
- Bitrate Limitation: The demo only provides 4 different settings of bitrate for each Encoder Model by two switches on the FPGA board. You can set any bitrate in valid range by formal version.
- Resolution Limitation: The demo supports only two resolutions 1920x1080 and 1280x720. The formal version supports resolution from 176x144 to 4000x4000 or even larger.
- GOP Size: evaluation version is limited to 60 for I+P or 1 for I-only, formal version can be any value in valid range.
- Error Recovery: The demo doesn't provide automatic resume on subsequent errors:
    - Input Video Signal Interrupt, such as disconnect and reconnecting input HDMI cable
    - Entropy FIFO overflow

  The formal version provides tools to resume from those errors.

2. REQUIREMENTS

1. FPGA Development boards:

A.	TED inrevium TB-6S-LX150T	The main development board
B.	TED inrevium TB-FMCL-HDMI	The HDMI daughter board
C.	TED inrevium TB-OP-LAN	The GigaEthernet PHY daughter board
D.	TED inrevium TB-FMCL-TYPEA	The interface conversion board to install TB-OP-LAN on TB-6S-LX150T

Note: TB-6S-LX150T and TB-FMCL-HDMI are included in the Spartan-6 FPGA Consumer Video Kit by TED (CVK).

2. A video source able to output HDMI/DVI signal at 1920x1080p (30, 25 or 24Hz) or 1280x720p (60, 30, 25 or 24Hz).

3. A HDMI cable which complies with HDMI 1.3 standard.

4. A PC or laptop with subsequent configuration:

   - CPU frequency should be at least 1.6GHz
   - A Gigabit Ethernet adapter
   - Windows XP or Windows Vista
   - Optional, a high resolution display (1920x1200 or 1920x1080). It can be either laptop built-in screen or external monitor/TV with resolution with compatible video card on PC

   Thinkpad laptop T60, T61, T400, T500, X60, X61 are tested in Jointwave laboratory, all work well.

5. A 1 to 3 meter long CAT6 Ethernet cable to connect the FPGA board and the PC. The quality of cable and its RJ45 head is important, because the Demo doesn't have error correcting mechanism such as TCP in Ethernet transmission. A high quality cable is essential to guarantee that 100% Ethernet packets are transmitted and received successfully.

3. SETUP AND RUN PROCEDURE

1. Contact Jointwave to get the demo suite, which comprises of:

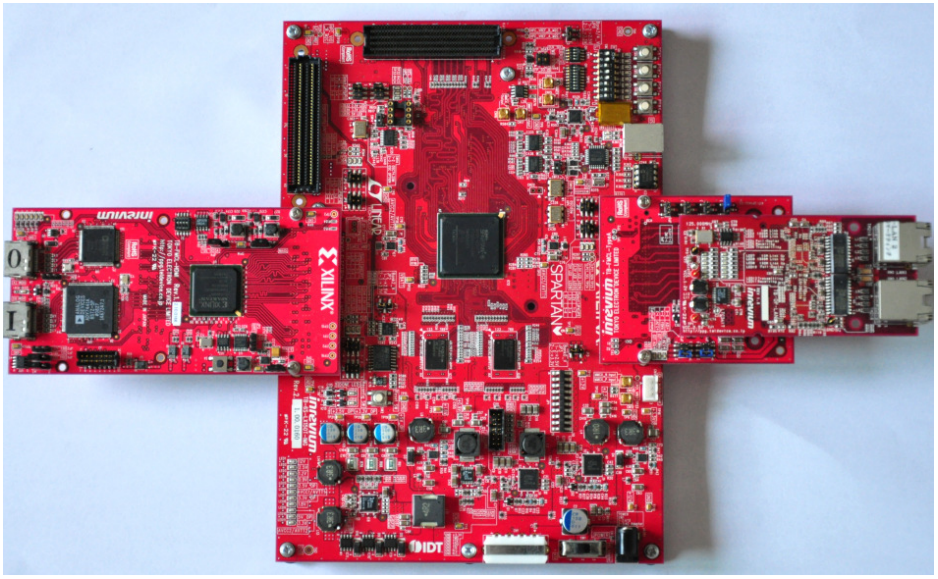
   A. A FPGA image file, in Xilinx BIT format.
   B. Demo Supporting Package
      Following files are included in Jointwave demo supporting package:

      win_pcap_XXXX.exe
      vcredit_x86.exe
      etherdump.exe
      mplayer.exe

2. Install winpcap_XXXX.exe in Jointwave demo supporting package onto your PC

3. Install vcredist_x86.exe in Jointwave demo supporting package onto your PC

4. Install daughter board on TB-6S-LX150T as following picture:



   A. Install TB-FMCL-HDMI on TB-6S-LX150T CN6 port

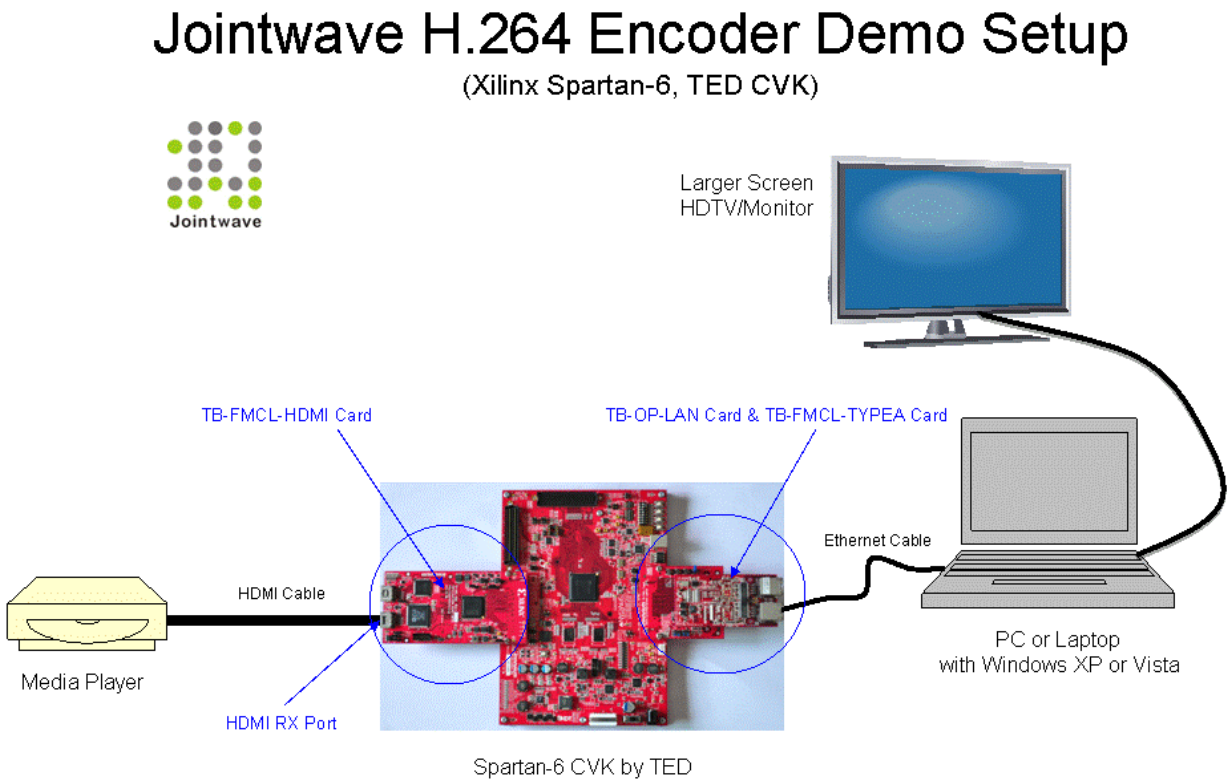
   B. Install TB-OP-LAN on TB-FMCL-TYPEA, then install TB-FMCL-TYPEA on TB-6S-LX150T CN5 Port

      Set voltage of TB-OP-LAN to 3.3V by following jumper settings on TB-FMCL-TYPEA

JP1	1-2
JP2	1-2
JP3	2-3
All other Jumpers	Open

5. Connect video source, FPGA board and PC together as following picture.

   Note: The Ethernet cable must be connected to CN3 (LAN2) port of TB-OP-LAN



6. Set *DIPSWITCH SW3* on FPGA board according to your resolution, bitrate and other parameters. Refer to Chapter 4 for details.

7. Power up the FPGA board and program the BIT file you want to run by using *Xilinx iMPACT* software. Since the TB-6S-LX150T all don't reset after programming, a reset is required after programming. Button *PSW1* does the resetting.

8. Power up your video source – which could be a blue-ray player or hard disk HD player. It's better to be powered up the player after the FPGA board is on, because some players require correct EDID information from the HDMI daughter board to set the HDMI output in appropriate mode.

9. Open a command prompt window and run etherdump.exe in Jointwave demo supporting package, it will list all the network cards and prompt you to select the correct device, as shown in following example (Note: If your operating system is Windows Vista, you need to run a command prompt windows "*as Adminstrator*" even you are the administrator, then run etherdump.exe in it):

   No adapter selected: printing the device list:
   1. \Device\NPF_{9ADFE0B9-683F-446A-A962-EAEB5A2062D8}

```
    (MS Tunnel Interface Driver)
2. \Device\NPF_{115E1410-4E51-4B9C-B62D-566359FCF6A5}
    (Intel(R) PRO/1000 PL Network Connection)
3. \Device\NPF_{CAA92102-B1D4-4C95-AE49-ECBEC31B2B4A}
    (Microsoft)
Enter the interface number (1-3): 2
```

Select the correct device, in the example it's 2.

Next the program will prompt “Enter the dump-file-path:”. Just input the file name to dump the h.264 stream, such as "a.264". (Note: If the BIT file name contains “ts” string which means it’s an h264+ts demo, the suffix of the stream name should be “.ts”).

Then the program will prompt “Enter how many Ethernet packets per dump (valid range 1 to 16384):”. Refer to following table to input an appropriate value.

Target Bitrate (Mbps)	Suggested Packets Per Dump value
4 and lower	512
8	1024
16	2048
32	4096
64	8192
128 and larger	16384

Tip: After first running, you can combine the inputted answers to create a .bat file, for example:

File *myetherdump.bat:*

```
etherdump \Device\NPF_{115E1410-4E51-4B9C-B62D-566359FCF6A5} a.264 1024
```

Then you just type the command “myetherdump” to run it.

10. After a few seconds, you can see following text is printing and scrolling on the command windows:

```
0 * 1048576 S00 PktErr= 0
1 * 1048576 S01 PktErr= 0
2 * 1048576 S02 PktErr= 0
…….
```

Every time, the program etherdump.exe dumps “PacketPerDump” number of 1024bytes Ethernet packets onto the hard disk and prints one line text on command window.

Now you can play the dumped file by using mplayer.exe in Jointwave demo supporting package. If your file name is a.264 and the video source's frame rate is 30, the mplayer.exe command line will be:

```
mplayer a.264 -fps 30
```

Or if the BIT name contains “ts”, it’s a h264+ts demo, the command line will be:

```
mplayer -demuxer lavf a.ts
```

Note: If PktErr doesn’t equal to 0, it means some Ethernet packets are already lost, thus mplayer will report error and some video frames might be partially corrupted too. The Demo doesn’t have error correcting mechanism such as TCP in Ethernet transmission, but we designed etherdump.exe to make the possibility of packet loss infinitesimal.

Disabling SpeedStep of CPU on laptop helps to reduce packet loss further. It can be done in BIOS or by some software, e.g. RightMark CPU.

11. Refer to Chapter 4 for changing encoding parameters and observing status and error of the encoder by switches and LEDs on the FPGA board.

12. You can observe the live bitrate chart by Windows Task Manger.

    Setup 1. Open Windows Task Manger, then switch to page “Networking”.
    Setup 2. Menu View → Network Adapter History → Bytes Received (Yellow).

4. FPGA BOARD CONFIGURATIONS

4.1. Reset

On TB-6S-LX150T board, button **PSW1** resets the Demo.

4.2. Configuring the Encoder by DIP SWITCH

On TB-6S-LX150T board, The DIPSW **SW3** configures the parameters of the Encoder:

SW3-1

1	Activate the encoder
0	Deactivate the encoder

SW3-2

1	Constant Bitrate Mode rate control (CBR)
0	Const QP Mode rate control (CQR)

SW3-4, SW3-3 in CBR Mode (when SW3-2 == 1), Bitrate Configuration (Mbps)

The following table shows the output bitrate (in Mbps) for each board with different inputs.

Note 1: The encoder will adapt to the input frame rate if it's within the maximum limit, and the bitrate is proportional to the FPS. For example, SW3-4,SW3-3=1,0 on TB-6S-LX150T running E640 with 720p@60fps input, the output is 16Mbps; when the input changes to 720p@30fps, the output will be 8Mbps.

Note 2: These tables show the bitrate for standard demo. If you get a customized demo BIT, please refer to the email or readme file come with it for bit rate setting.

a) **1080p@30fps** input

SW3-4	SW3-3	E240/E340/E540	E440/E640
0	0	64	50
0	1	32	16
1	0	16	8
1	1	8	4

b) **720p@60fps** input

SW3-4	SW3-3	E240/E340/E540	E440/E640
0	0	128	Invalid
0	1	64	32
1	0	32	16
1	1	16	8

SW3-4, SW3-3 in CQR Mode (SW3-2 == 0)

SW3-4	SW3-3	QP

0	0	16
0	1	24
1	0	32
1	1	40

SW3-5

1	Invert DVI V-sync signal's polarity
0	Keep DVI V-sync signal's polarity

SW3-6 (E540/E640 Only)

1	I + P frame
0	I frame only *(note: CBR mode is unavailable in current E5X0/E6X0 demo's I-Only mode)*

SW3-7 and SW3-8 are not used.

4.3. LED

LED0	On: DDR2 controller is initialized successfully Off: DDR2 controller doesn't work
LED1	On: ERROR, Entropy FIFO overflows Off: good state
LED2	On: ERROR, Sensor's data rate is higher than the Encoder's encoding capacity Off: good state
LED3	Blinking: Encoder is sending output byte stream Off: No output from Encoder
LED4	connect to V-sync signal of video inputting interface
LED5	connect to Data Enable (or Href) signal of video inputting interface
LED6	connect to All Data signals' OR of video inputting interface
LED7	*Note: For H.264+TS demo only, If the BIT file name contains "ts" string, it's a H.264+TS demo file*. On: TS Mux is working Off: TS Mux is not working Button USER_PB1 is used to switch on/off TS Mux.
TX (Ethernet)	On to indicated encoded H.264 stream is outputting from the Gigabit Ethernet chip

5. TROUBLE SHOOTING

Problem	Solution
Ethernet TX LED is not on	1. Check if the video source is playing 2. Check if the video source is connected to the Bitec DVI daughter board correctly 3. Check if the Bitec DVI daughter board is installed on the FPGA board tightly 4. Check if SW0 of USER DIPSWITCH is set to ON 5. If the problem still exists, try to toggle SW6 of USER DIPSWITCH to change DVI vsync signal's polarity